

AMENDMENT UNDER 37 C.F.R. § 1.116

U.S. Appln. No.: 09/404,313

Attorney Docket No.: Q55935

REMARKS

General Matters

Claims 1-13 are all the claims pending in the application, and all stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over the combined teachings of three references.

The Examiner has not yet returned an acknowledged PTO-1449 of any of the Information Disclosure Statements filed on September 24, 1999, June 29, 2000, November 20, 2001, October 24, 2002, and December 16, 2002. The Examiner is respectfully requested to comply with the MPEP in this regard and return initialed copies of the PTO forms 1449, or else explain why none of the references submitted by Applicant have been considered.

Drawings

Applicant thanks the Examiner for acknowledging and approving the proposed drawing amendment filed on December 10, 2003. The Examiner objects to the drawings for the reasons set forth on page 2 of the Office Action. Specifically, the Examiner asserts that the reference sign "14" mentioned in the specification are not depicted in the.

Applicant has amended the figures such that the reference signs identified by the Examiner are included within the figures. The corrected drawings are submitted and now comply with 37 C.F.R. § 1.84(p)(5). Accordingly, Applicant respectfully requests that the objection to the drawings be withdrawn.

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Prior art rejections.

Claims 1,2,5,6, and 8-11 stand **finally** rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokoyama et al. (U.S. Patent No. 5,303,344, hereafter "Yokoyama") in view of Albal et al. (U.S. Patent No. 4,821,265, hereafter "Albal") in further view of Stoner et al. (U.S. Patent No. 6,052,383, hereafter "Stoner"). Claims 1, 2, 5, 6, 8, 9, and 11 are independent.

Independent claim 1

Applicant respectfully traverses this rejection, first with respect to independent claim 1, in view of its requirements for:

1. a packet memory for storing the entire packet; and
2. a shared memory for storing part of each packet of the packet data used in processes of a lower layer processing portion and a higher layer processing portion,
3. the lower layer processing portion and the higher layer processing portion accessing the same memory space of said shared memory through physically different memory buses.

In making this rejection, the Examiner asserts that Yokoyama discloses the required "shared memory for storing part of each packet" by virtue of its memory 30, but acknowledges that Yokoyama fails to disclose a packet memory for storing the entire packet. The Examiner cites Albal to make up for this particular deficiency. The examiner acknowledges that even the combined teachings of Yokoyama and Albal do not teach or suggest that the lower layer and higher layer processing portions access the shared memory through separate buses. The Examiner cites Stoner to compensate for this deficiency.

However, the above prior-art references do not contain any suggestion (express or implied) that they be combined, or that they be combined in the manner suggested. Yokoyama

discloses a buffer memory for storing the data received by the MAC LSI (see col.4, ln. 40-43, Yokoyama). Albal teaches a queue circuit which is coupled to a common Processor Bank which is shared by all of the DSLs via a layer 1 layer 2 receive bus and a layer 1 layer 2 transmit bus (see col. 6, ln. 10-15, Albal). Albal uses the queue circuit to facilitate concurrent processing of multiple D Channel messages in ISDN. There is no suggestion that Yokoyama would use any such queue circuit in addition to the buffer memory already taught in Yokoyama. Such an addition to Yokoyama is unnecessary.

Each reference is complete and functional in itself, so there would be no reason to use parts from or add or substitute parts to Yokoyama, Albal, or Stoner. The above references each aim to achieve faster packet processing. But they each do this by taking mutually exclusive paths to reach different solutions to a similar problem. Yokoyama teaches communication control equipment including a computer interface connected to a host computer, a network interface connected to a network for transmission and reception of data between the network interface and the network, and a buffer memory connected between these interfaces for temporarily storing communication data (see col. 1, ln. 65 - col. 2, ln. 5, Yokoyama). Yokoyama already contains a buffer memory so adding a packet memory in the form of a queue circuit as in Albal would add unnecessary bulk to the invention of Yokoyama. Combining the Albal and Stoner with Yokoyama would be cumbersome since Yokoyama is capable of performing high speed processing without any additions. The combination suggested requires a series of separate, awkward combinative steps that are too involved to be considered obvious.

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While Stoner teaches two separate and distinct ports on the memory (*see*, col. 4, ln. 43-46, Stoner), Yokoyama includes a main processor, a main memory, and a system bus connecting the main processor and the main memory (*see* col. 4, ln. 32-34, Figure 52, Yokoyama). There is no suggestion that allowances would be made for additional memory be placed in Yokoyama. Those skilled in the art would find it physically impossible to combine Yokoyama and Albal in the manner suggested to make room for this additional memory. Additionally, it would be necessary to make additional modifications, not taught in the prior art, in order to combine the references in the manner suggested.

The Examiner has found in Yokoyama, in Albal, and in Stoner evidence that the claims do not recite any brand new components, but no evidence whatever that the unique combination of elements recited in claim 1 would have been obvious. Applicant finds no objective benefit to including an additional Albal-type memory in the Yokoyama circuit,. There is no need for it. What would such a memory do? Where would it be placed? How would it be controlled? The prior art provides no answer to any of these questions. The combination of elements suggested by the Examiner is illogical, unsupported by the evidence, and does not in any way flow "obviously" from the prior art. Such a combination is only logical once Applicant's own disclosure has been revealed, and therefore constitutes impermissible hindsight reconstruction.

Applicant therefore respectfully requests the Examiner's reconsideration and withdrawal of the above 35 U.S.C. § 103(a) rejection of claim 1. As claim 4 further depends on independent claim 1, Applicant also respectfully submits that this claim is also allowable at least by reason of its dependence.

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Independent claim 2.

Applicant respectfully traverses the 35 U.S.C. § 103(a) rejection with respect to independent claim 2, which requires:

4. a packet memory for storing the entire packet; and
5. a shared memory as a multi-port memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer,
6. the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of said shared memory, ...

The prior art references do not contain any suggestion (express or implied) that they be combined, or that they be combined in the manner suggested to result in the claimed invention.

Yokoyama teaches a buffer memory for storing transmitted data and receiving data (*see* col 4, ln. 32-35, Yokoyama). This reference is complete and functional in itself, so there would be no reason to use parts from Albal such as the queue circuit (*see* col. 6, ln. 1-11, Albal) or added or substitute parts to this reference.

Those skilled in the art would find it physically cumbersome to combine the references of Yokoyama, Albal, and Stoner in the manner suggested. Also, the combination suggested requires a series of separate, awkward combinative steps to arrive at the claimed invention's multi-port memory with layer 2 and 3 recommended by the Open System Interconnection reference model. Albal is completely functional without any additions such as the features of Stoner or Yokoyama. For example, Albal already uses a plurality of processors to handle layer 2 and layer 3 processes with general purpose processors (*see* col. 4, ln. 20-22, Albal). It is unnecessary to incorporate the separate busses disclosed in Stoner.

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Therefore, Applicant respectfully requests the Examiner's reconsideration and withdrawal of the above 35 U.S.C. § 103(a) rejection of claim 2 and its dependent claim 3.

Independent claims 5, 6, 8, 9, and 11.

The foregoing points made with respect to independent claims 1 and 2 are respectfully submitted to apply at least by analogy to the rejection of independent claims 5, 6, 8, 9, and 11 in view of the apparent similarities among these independent claims. For such analogous reasons, therefore, Applicant respectfully requests the Examiner also to reconsider and to withdraw the § 103 rejection of claims 5, 6, 8, 9, and 11, and also that of rejected dependent claim 10/11.

Allowable Subject Matter

Applicant gratefully notes the continued indication of allowable subject matter in claims 3-4, 7 and 12-13. These claims are objected to as being dependent upon a rejected base claim, but allowable if appropriately rewritten in independent form. In view of the comments and evidence above, however, Applicant respectfully requests of the Examiner the allowance of these claims in their present form.

Conclusion and request for telephone interview

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

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The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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